FIG.1

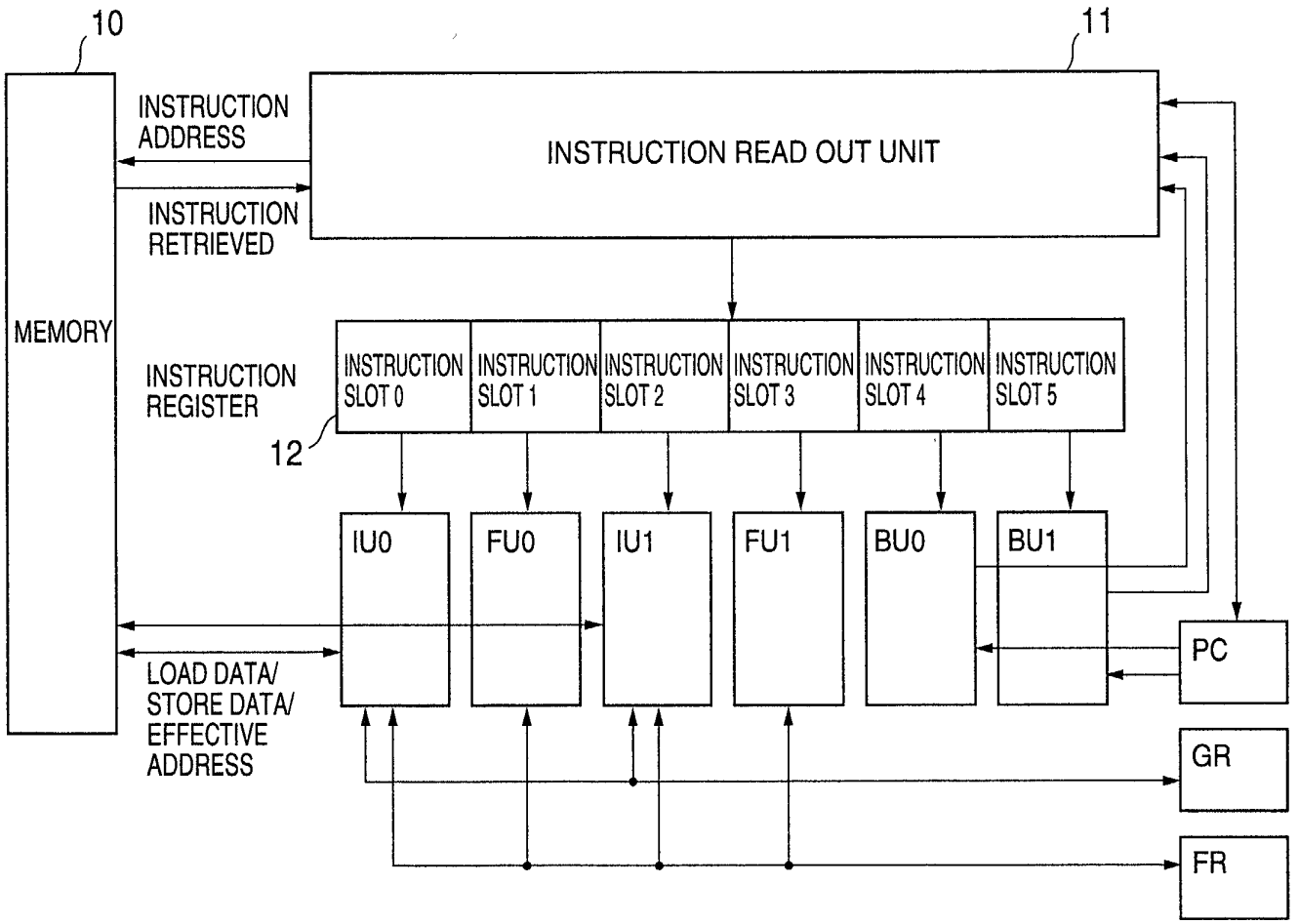

10
11
MEMORY
INSTRUCTION ADDRESS
INSTRUCTION RETRIEVED
INSTRUCTION READ OUT UNIT
INSTRUCTION REGISTER
12
INSTRUCTION SLOT 0
INSTRUCTION SLOT 1
INSTRUCTION SLOT 2
INSTRUCTION SLOT 3
INSTRUCTION SLOT 4
INSTRUCTION SLOT 5
IU0
FU0
IU1
FU1
BU0
BU1
PC
GR
FR
LOAD DATA/
STORE DATA/
EFFECTIVE ADDRESS

FIG. 2

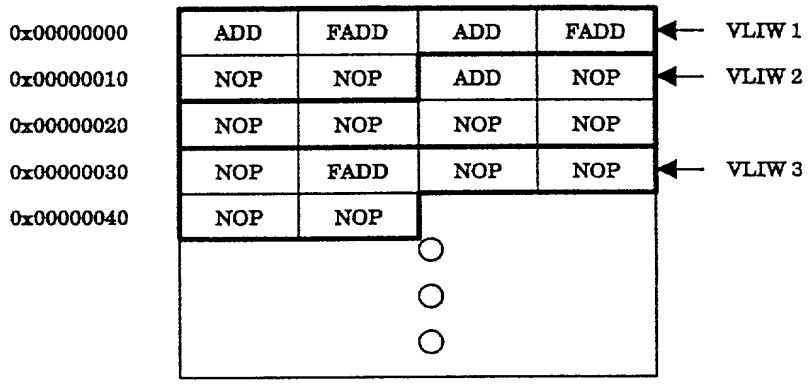

0x00000000
0x00000010
0x00000020
0x00000030
0x00000040
ADD
FADD
ADD
FADD
NOP
NOP
ADD
NOP
NOP
NOP
NOP
NOP
NOP
FADD
NOP
NOP
NOP
NOP
VLIW 1
VLIW 2
VLIW 3

FIG. 3

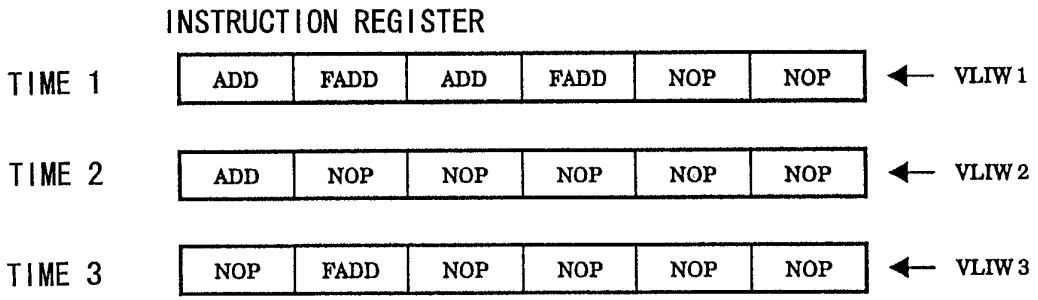

INSTRUCTION REGISTER
TIME 1
ADD
FADD
ADD
FADD
NOP
NOP
VLIW 1
TIME 2
ADD
NOP
NOP
NOP
NOP
NOP
VLIW 2
TIME 3
NOP
FADD
NOP
NOP
NOP
NOP
VLIW 3

FIG.4

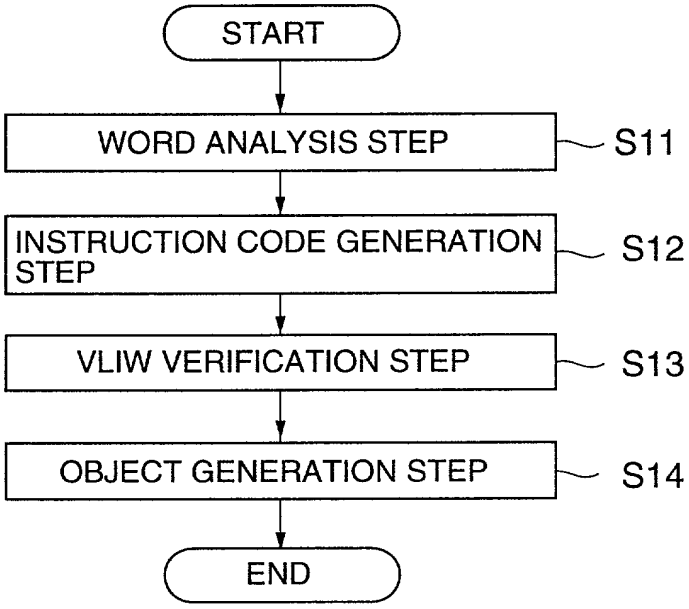

START
WORD ANALYSIS STEP
S11
INSTRUCTION CODE GENERATION STEP
S12
VLIW VERIFICATION STEP
S13
OBJECT GENERATION STEP
S14
END

FIG.5

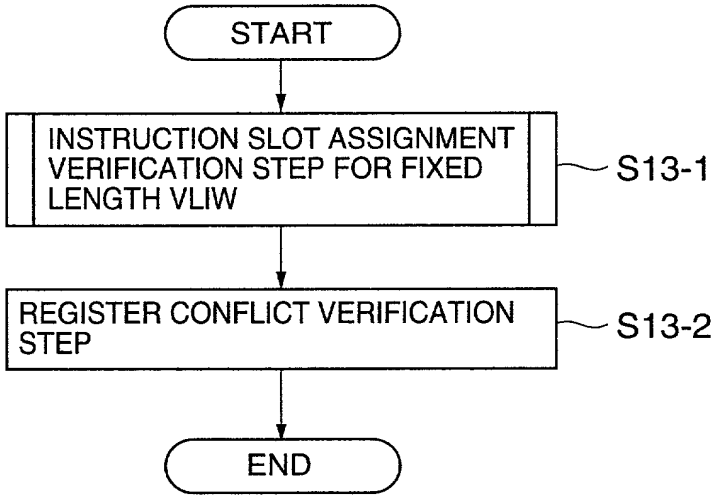

START
INSTRUCTION SLOT ASSIGNMENT VERIFICATION STEP FOR FIXED LENGTH VLIW
S13-1
REGISTER CONFLICT VERIFICATION STEP
S13-2
END

FIG.6

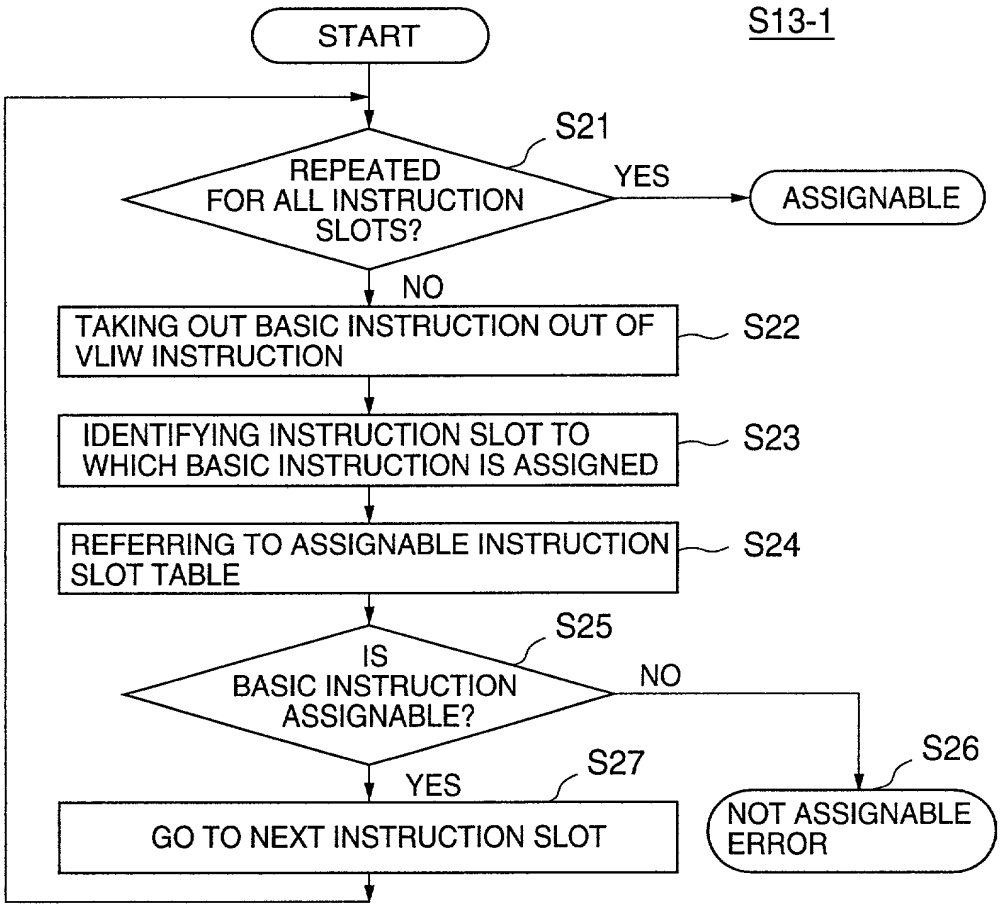

START
S13-1
S21
REPEATED FOR ALL INSTRUCTION SLOTS?
YES
ASSIGNABLE
NO
TAKING OUT BASIC INSTRUCTION OUT OF VLIW INSTRUCTION
S22
IDENTIFYING INSTRUCTION SLOT TO WHICH BASIC INSTRUCTION IS ASSIGNED
S23
REFERRING TO ASSIGNABLE INSTRUCTION SLOT TABLE
S24
S25
IS BASIC INSTRUCTION ASSIGNABLE?
NO
S26
NOT ASSIGNABLE ERROR
YES
S27
GO TO NEXT INSTRUCTION SLOT

FIG.7

BASIC INSTRUCTION	INSTRUCTION SLOT					
	SLOT 0	SLOT 1	SLOT 2	SLOT 3	SLOT 4	SLOT 5
ADD	○	—	○	—	—	—
FADD	—	○	—	○	—	—
BRA	—	—	—	—	○	○

○ : ASSIGNABLE

— : NOT ASSIGNABLE

FIG.8

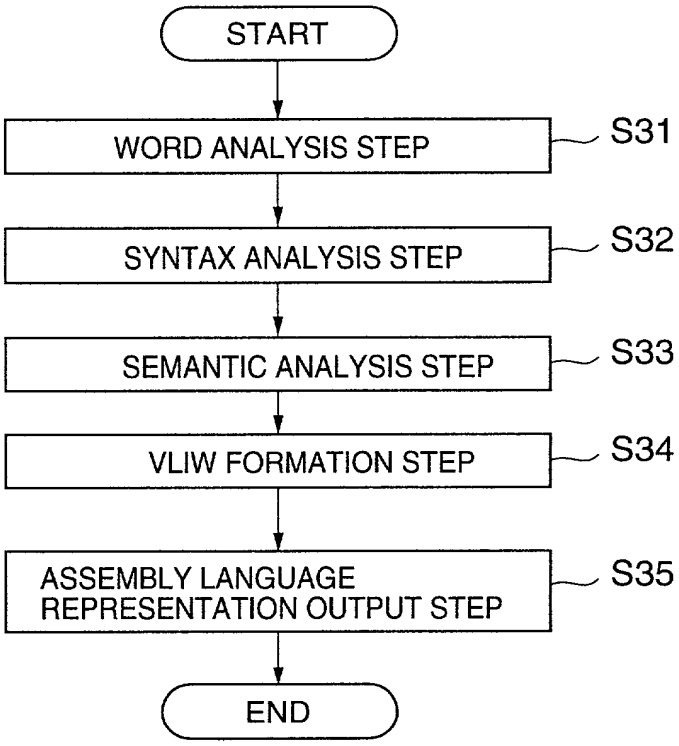
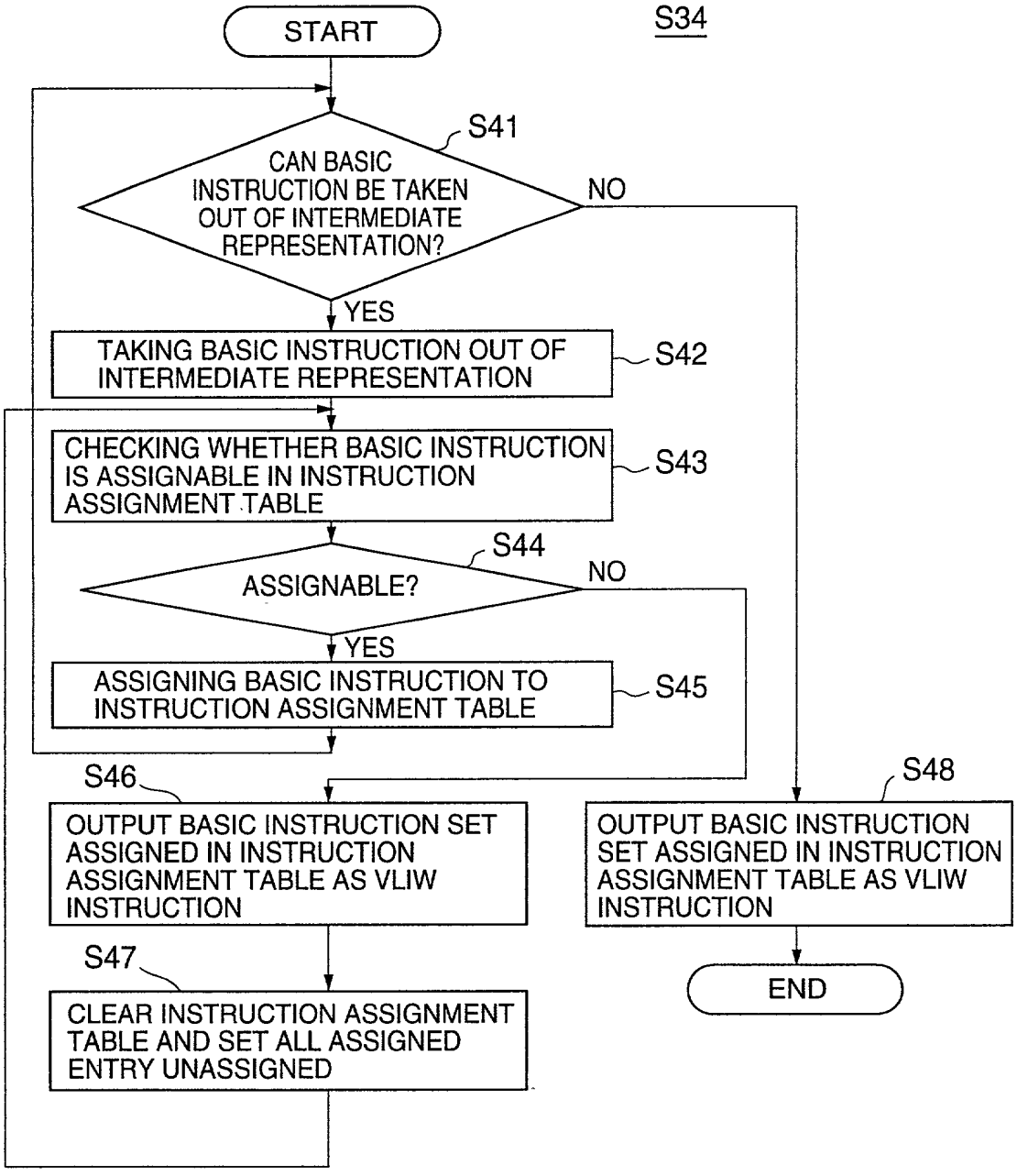

START
WORD ANALYSIS STEP
S31
SYNTAX ANALYSIS STEP
S32
SEMANTIC ANALYSIS STEP
S33
VLIW FORMATION STEP
S34
ASSEMBLY LANGUAGE REPRESENTATION OUTPUT STEP
S35
END

FIG.9



EP 0 954 794 A1

FIG.10

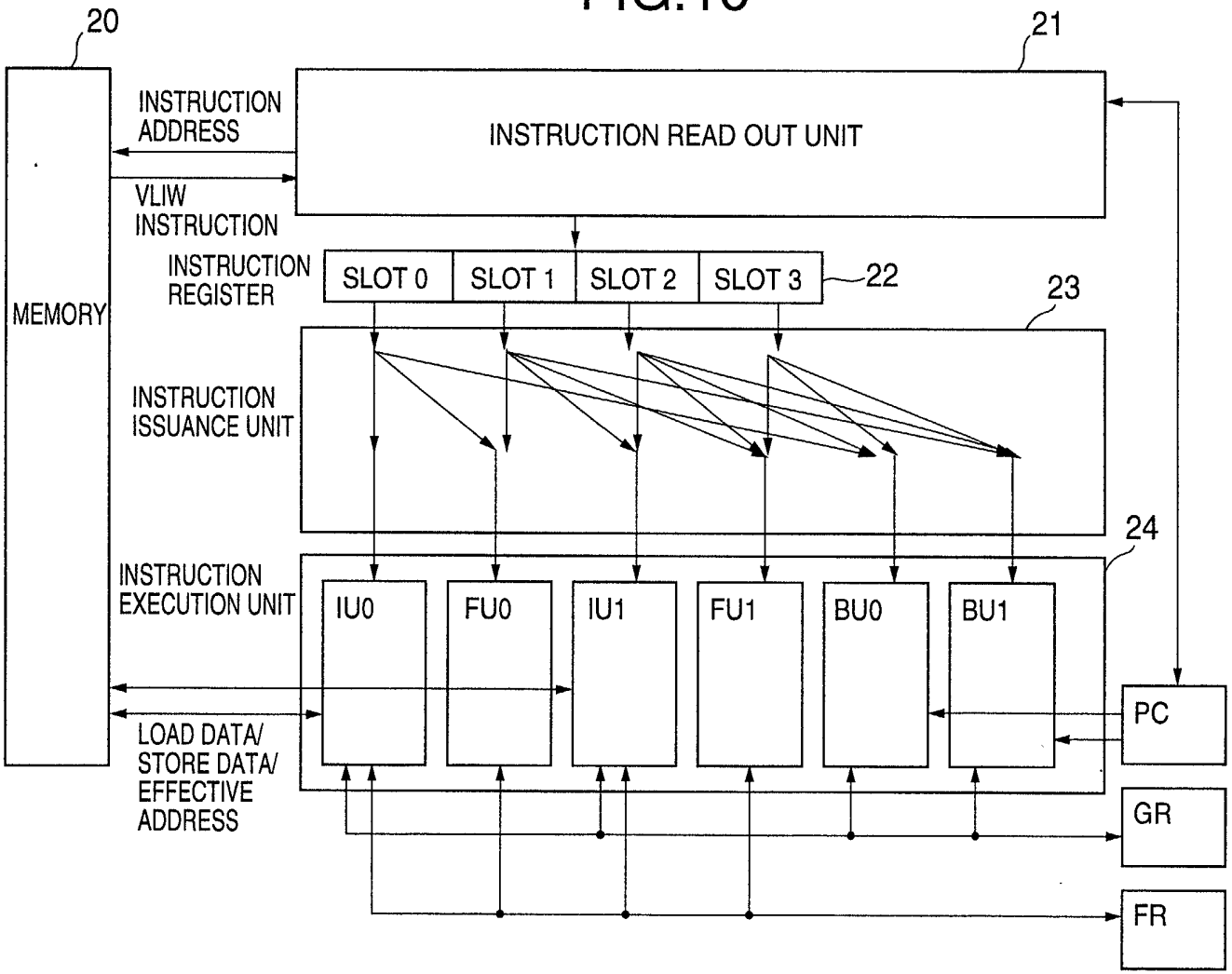

20
21
MEMORY
INSTRUCTION ADDRESS
VLIW INSTRUCTION
INSTRUCTION READ OUT UNIT
INSTRUCTION REGISTER
SLOT 0
SLOT 1
SLOT 2
SLOT 3
22
23
INSTRUCTION ISSUANCE UNIT
24
INSTRUCTION EXECUTION UNIT
IU0
FU0
IU1
FU1
BU0
BU1
PC
GR
FR
LOAD DATA/ STORE DATA/ EFFECTIVE ADDRESS

FIG.11

INSTRUCTION SLOT 0	INSTRUCTION SLOT 1	INSTRUCTION SLOT 2	INSTRUCTION SLOT 3
I0	F0	I1	F0
I0	F0	I1	B0
I0	F0	I1	
I0	F0	I1	B0
I0	F0	F1	
I0	F0	F1	B0
I0	F0	B0	B1
I0	F0	B0	
I0	F0		
I0	I1	B0	B1
I0	I1	B0	
I0	I1		
F0	F1	B0	B1
F0	F1	B0	
F0	F1		
I0	B0	B1	
I0	B0		
I0			
F0	B0	B1	
F0	B0		
F0			
B0	B1		
B0			

FIG.12

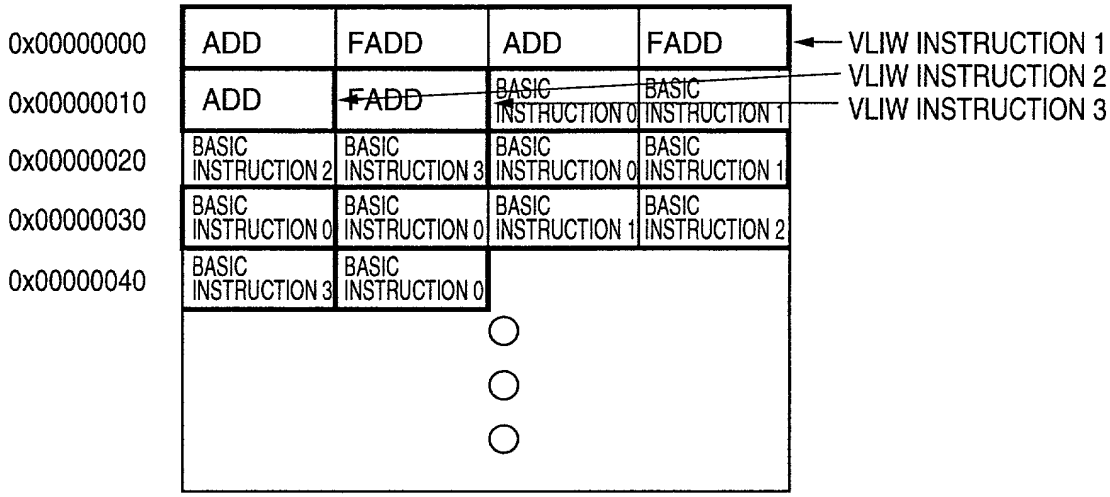

0x00000000
0x00000010
0x00000020
0x00000030
0x00000040
ADD
FADD
ADD
FADD
ADD
FADD
BASIC INSTRUCTION 0
BASIC INSTRUCTION 1
BASIC INSTRUCTION 2
BASIC INSTRUCTION 3
BASIC INSTRUCTION 0
BASIC INSTRUCTION 1
BASIC INSTRUCTION 0
BASIC INSTRUCTION 0
BASIC INSTRUCTION 1
BASIC INSTRUCTION 2
BASIC INSTRUCTION 3
BASIC INSTRUCTION 0
VLIW INSTRUCTION 1
VLIW INSTRUCTION 2
VLIW INSTRUCTION 3

FIG.13

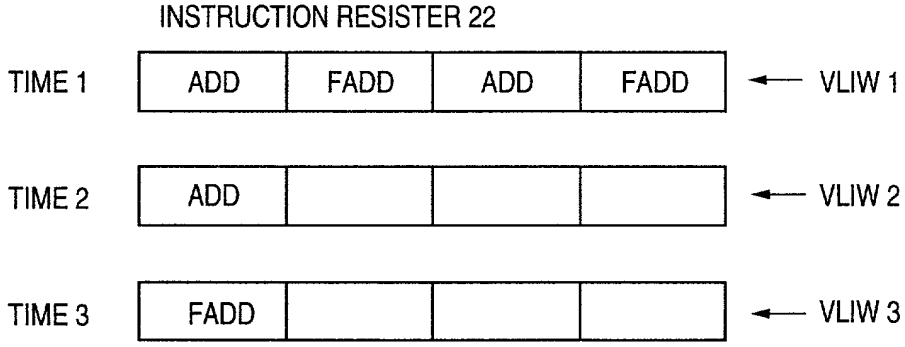

INSTRUCTION RESISTER 22
TIME 1
TIME 2
TIME 3
ADD
FADD
ADD
FADD
ADD
FADD
VLIW 1
VLIW 2
VLIW 3

FIG.14

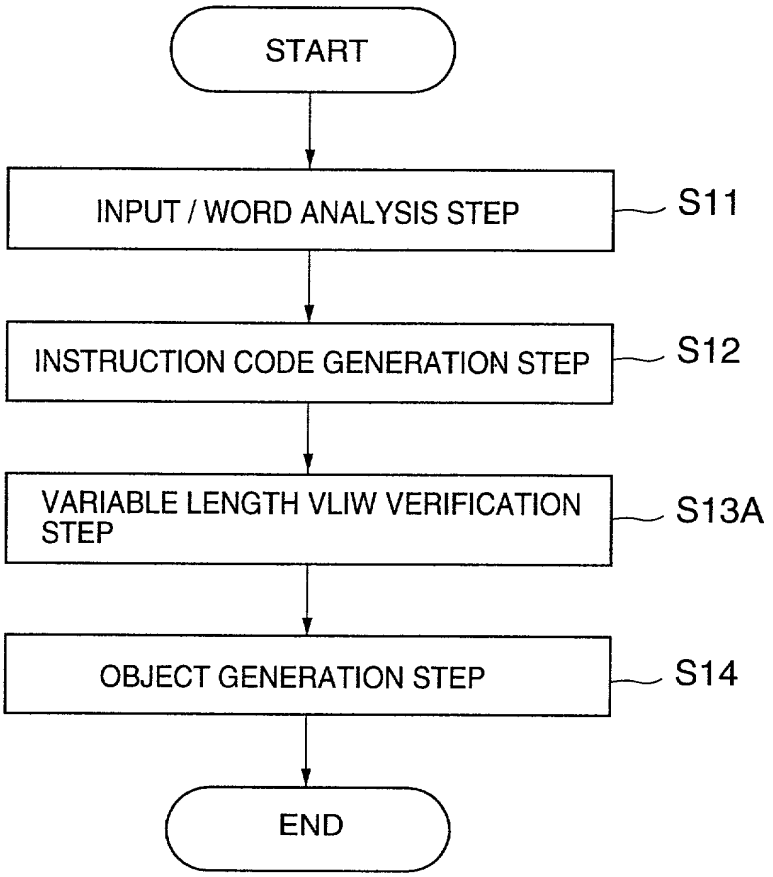

START
INPUT / WORD ANALYSIS STEP
S11
INSTRUCTION CODE GENERATION STEP
S12
VARIABLE LENGTH VLIW VERIFICATION STEP
S13A
OBJECT GENERATION STEP
S14
END

FIG.15

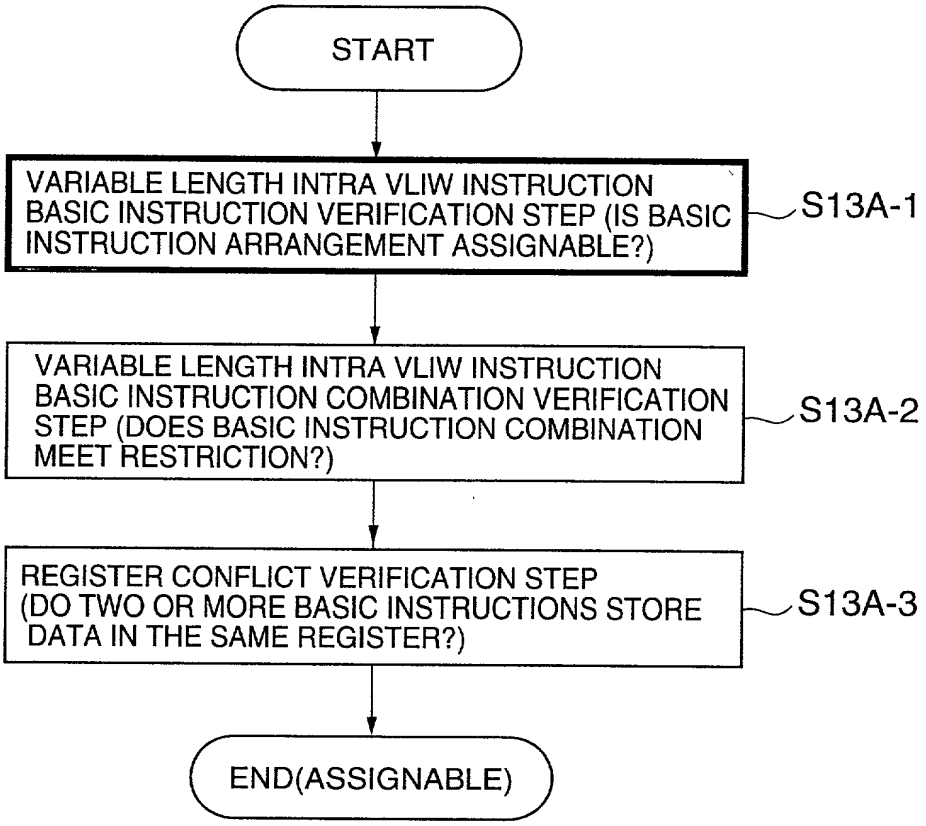

START
VARIABLE LENGTH INTRA VLIW INSTRUCTION BASIC INSTRUCTION VERIFICATION STEP (IS BASIC INSTRUCTION ARRANGEMENT ASSIGNABLE?)
S13A-1
VARIABLE LENGTH INTRA VLIW INSTRUCTION BASIC INSTRUCTION COMBINATION VERIFICATION STEP (DOES BASIC INSTRUCTION COMBINATION MEET RESTRICTION?)
S13A-2
REGISTER CONFLICT VERIFICATION STEP (DO TWO OR MORE BASIC INSTRUCTIONS STORE DATA IN THE SAME REGISTER?)
S13A-3
END(ASSIGNABLE)

FIG.16

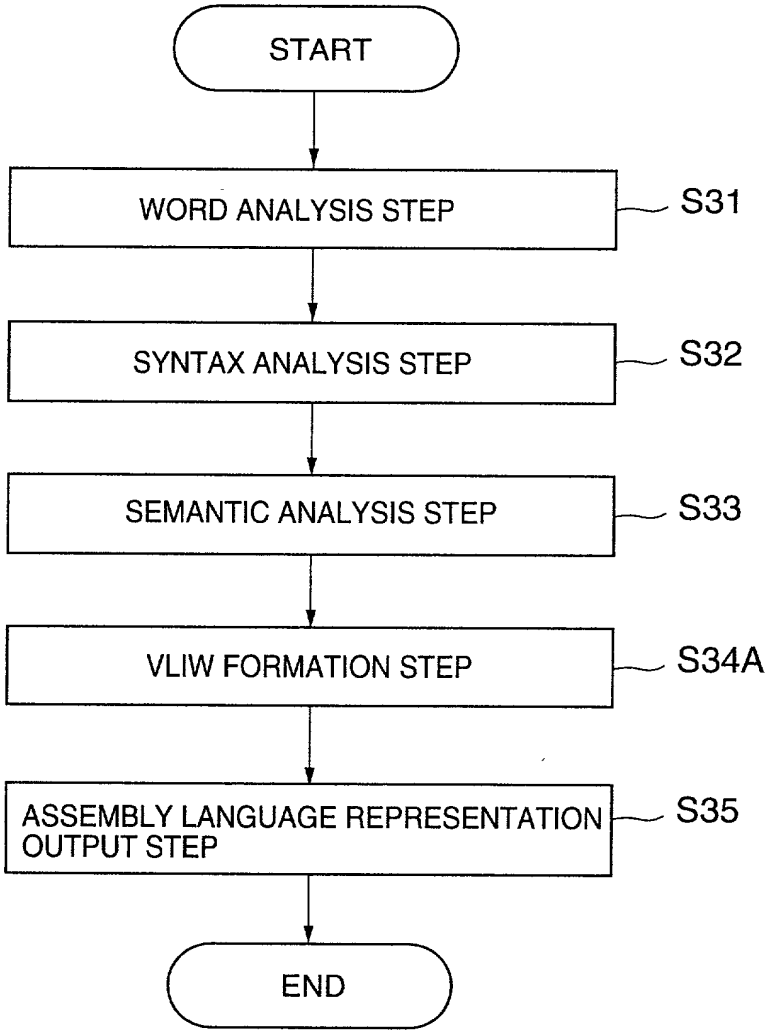

START
WORD ANALYSIS STEP
S31
SYNTAX ANALYSIS STEP
S32
SEMANTIC ANALYSIS STEP
S33
VLIW FORMATION STEP
S34A
ASSEMBLY LANGUAGE REPRESENTATION OUTPUT STEP
S35
END

FIG.17

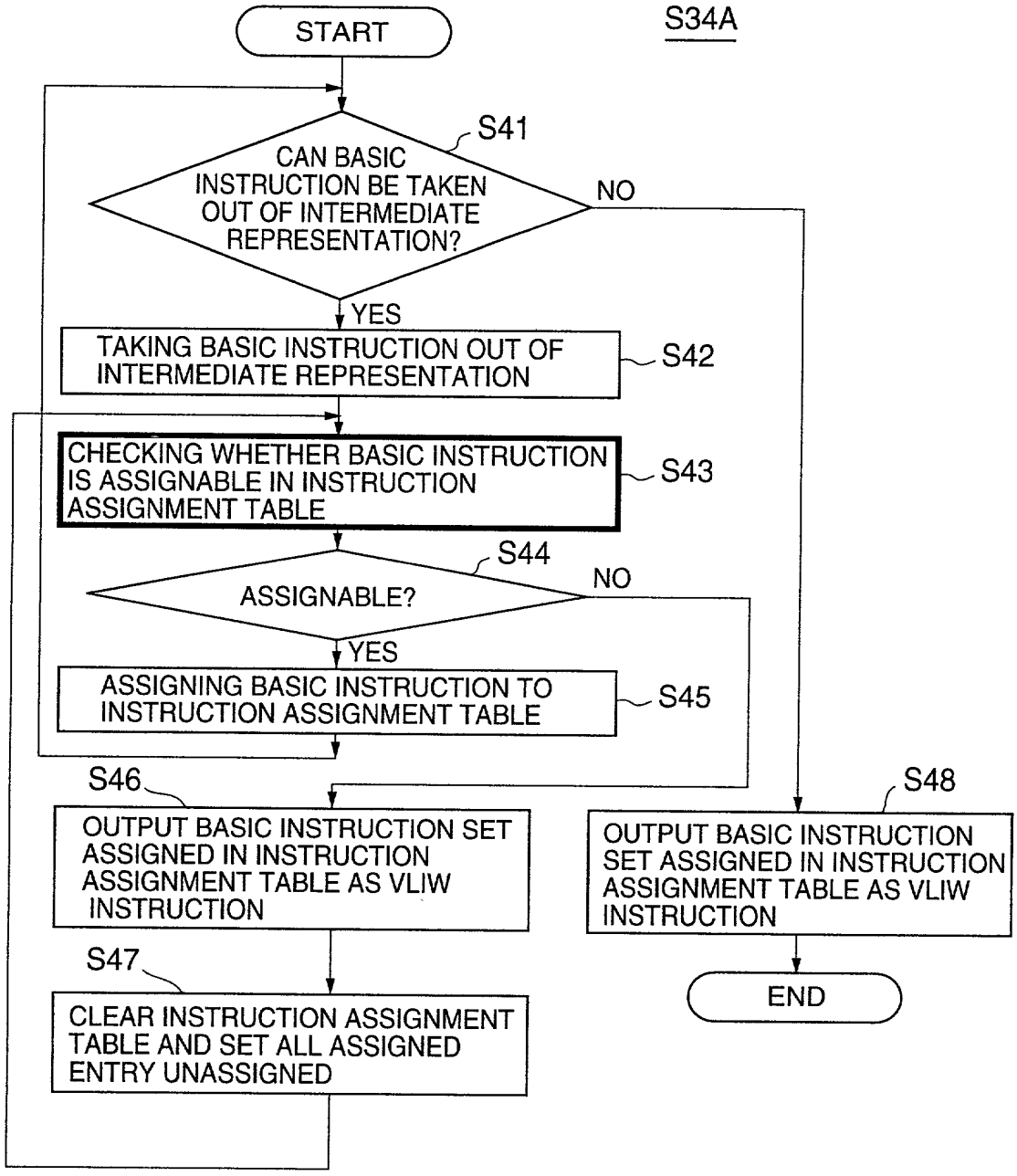

S34A
START
S41
CAN BASIC INSTRUCTION BE TAKEN OUT OF INTERMEDIATE REPRESENTATION?
NO
YES
TAKING BASIC INSTRUCTION OUT OF INTERMEDIATE REPRESENTATION
S42
CHECKING WHETHER BASIC INSTRUCTION IS ASSIGNABLE IN INSTRUCTION ASSIGNMENT TABLE
S43
S44
ASSIGNABLE?
NO
YES
ASSIGNING BASIC INSTRUCTION TO INSTRUCTION ASSIGNMENT TABLE
S45
S46
OUTPUT BASIC INSTRUCTION SET ASSIGNED IN INSTRUCTION ASSIGNMENT TABLE AS VLIW INSTRUCTION
S47
CLEAR INSTRUCTION ASSIGNMENT TABLE AND SET ALL ASSIGNED ENTRY UNASSIGNED
S48
OUTPUT BASIC INSTRUCTION SET ASSIGNED IN INSTRUCTION ASSIGNMENT TABLE AS VLIW INSTRUCTION
END

FIG.18

BASIC INSTRUCTION	FUNCTIONAL UNIT CLASSIFICATION
ADD	IU
FADD	FU
BRA	BU

IU : EXECUTABLE BY INTEGER UNITS
FU : EXECUTABLE BY FLOATING UNITS
BU : EXECUTABLE BY BRANCH UNIT

FIG.19

LOGICAL INSTRUCTION SLOT	ASSIGNABLE FUNCTIONAL UNIT CLASSIFICATION		
	IU	FU	BU
0	○	—	—
1	—	○	—
2	○	—	—
3	—	○	—
4	—	—	○
5	—	—	○

○ : EXECUTABLE — : NOT EXECUTABLE

FIG.20

PHYSICAL INSTRUCTION SLOT	INSTRUCTION INFORMATION ASSIGNED
INSTRUCTION SLOT 0	—
INSTRUCTION SLOT 1	—
INSTRUCTION SLOT 2	—
INSTRUCTION SLOT 3	—

— : NOT ASSIGNED ○ : ASSIGNED

FIG.21

FUNCTIONAL UNIT	FUNCTIONAL UNIT NUMBER OF EACH FUNCTIONAL UNIT TO WHICH BASIC INSTRUCTION IS ASSIGNED (BIT PATTERN)			
	0	1	2	3
IU	—	—	—	—
FU	—	—	—	—
BU	—	—	—	—

○ : ASSIGNED — : NOT ASSIGNED

EP 0 942 360 A2

FIG.22

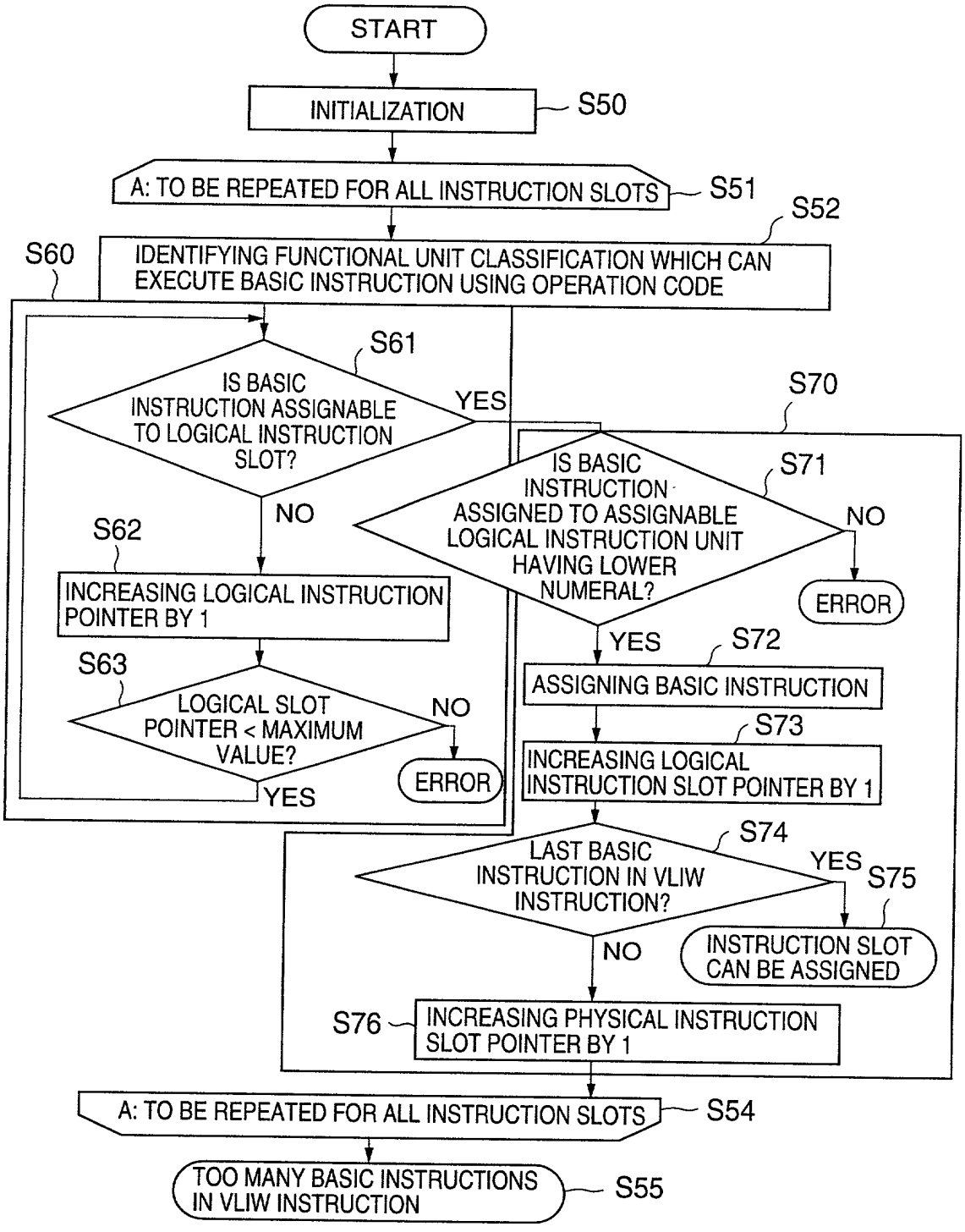

START
INITIALIZATION
S50
A: TO BE REPEATED FOR ALL INSTRUCTION SLOTS
S51
S52
S60
IDENTIFYING FUNCTIONAL UNIT CLASSIFICATION WHICH CAN EXECUTE BASIC INSTRUCTION USING OPERATION CODE
S61
IS BASIC INSTRUCTION ASSIGNABLE TO LOGICAL INSTRUCTION SLOT?
YES
NO
S62
INCREASING LOGICAL INSTRUCTION POINTER BY 1
S63
LOGICAL SLOT POINTER < MAXIMUM VALUE?
NO
ERROR
YES
S70
IS BASIC INSTRUCTION ASSIGNED TO ASSIGNABLE LOGICAL INSTRUCTION UNIT HAVING LOWER NUMERAL?
S71
NO
ERROR
YES
S72
ASSIGNING BASIC INSTRUCTION
S73
INCREASING LOGICAL INSTRUCTION SLOT POINTER BY 1
S74
LAST BASIC INSTRUCTION IN VLIW INSTRUCTION?
YES
S75
INSTRUCTION SLOT CAN BE ASSIGNED
NO
S76
INCREASING PHYSICAL INSTRUCTION SLOT POINTER BY 1
A: TO BE REPEATED FOR ALL INSTRUCTION SLOTS
S54
TOO MANY BASIC INSTRUCTIONS IN VLIW INSTRUCTION
S55

FIG.23

BASIC INSTRUCTION OPERATION CODE	FUNCTIONAL UNIT CLASSIFICATION	FUNCTIONAL UNIT NUMBER OF FUNCTIONAL UNIT CLASSIFICATION			
		0	1	2	3
ADD	IU	○	○	—	—
FADD	FU	○	○	—	—
BRA	BU	○	○	—	—

IU : EXECUTABLE BY INTEGER UNIT

FU : EXECUTABLE BY FLOATING UNIT

BU : EXECUTABLE BY BRANCH UNIT

○ : ASSIGNABLE

— : NOT ASSIGNABLE

FIG.24

LOGICAL INSTRUCTION SLOT	ASSIGNABLE FUNCTIONAL UNIT CLASSIFICATION			FUNCTIONAL UNIT NUMBER OF EACH FUNCTIONAL UNIT CLASSIFICATION			
	IU	FU	BU	0	1	2	3
0	○	—	—	○	—	—	—
1	—	○	—	○	—	—	—
2	○	—	—	—	○	—	—
3	—	○	—	—	○	—	—
4	—	—	○	○	—	—	—
5	—	—	○	—	○	—	—

○ : ASSIGNABLE

— : NOT ASSIGNABLE

FIG.25

BASIC INSTRUCTION	INSTRUCTION CATEGORY
ADD	I_1
DIV	I_2
FADD	F_1
BRA	B_1

I_1 : INTEGER CATEGORY 1

I_2 : INTEGER CATEGORY 2

F_1 : FLOATING CATEGORY 1

B_1 : BRANCH CATEGORY 1

FIG.26

LOGICAL INSTRUCTION SLOT	FUNCTIONAL UNIT CLASSIFICATION	BIT PATTERN OF FUNCTIONAL UNIT NUMBER OF EACH FUNCTIONAL UNIT CLASSIFICATION			
		0	1	2	3
I_1	IU	○	○	—	—
I_2	IU	○	—	—	—
F_1	FU	○	○	—	—
B_1	BU	○	—	—	—

○ : EXECUTABLE — : NOT EXECUTABLE

FIG.27

LOGICAL INSTRUCTION SLOT	ASSIGNABLE FUNCTIONAL UNIT CLASSIFICATION			BIT PATTERN OF FUNCTIONAL UNIT NUMBER OF EACH FUNCTIONAL UNIT CLASSIFICATION			
	IU	FU	BU	0	1	2	3
0	○	—	—	○	—	—	—
1	—	○	—	○	—	—	—
2	○	—	—	—	○	—	—
3	—	○	—	—	○	—	—
4	—	—	○	○	—	—	—
5	—	—	○	—	○	—	—

○ : EXECUTABLE — : NOT EXECUTABLE

2004.10.26 09:26:04

FIG.28

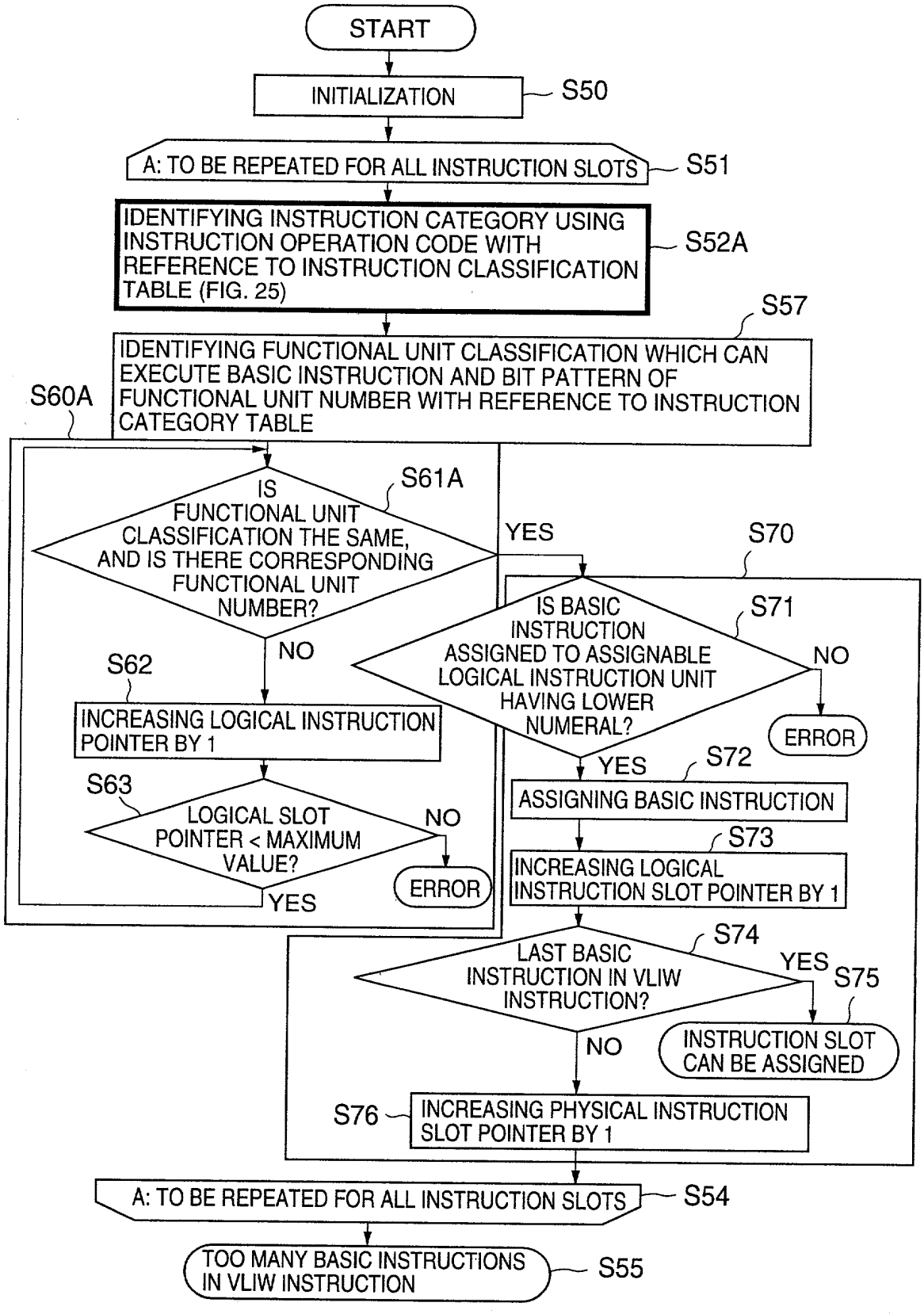

START
INITIALIZATION
S50
A: TO BE REPEATED FOR ALL INSTRUCTION SLOTS
S51
IDENTIFYING INSTRUCTION CATEGORY USING INSTRUCTION OPERATION CODE WITH REFERENCE TO INSTRUCTION CLASSIFICATION TABLE (FIG. 25)
S52A
S57
IDENTIFYING FUNCTIONAL UNIT CLASSIFICATION WHICH CAN EXECUTE BASIC INSTRUCTION AND BIT PATTERN OF FUNCTIONAL UNIT NUMBER WITH REFERENCE TO INSTRUCTION CATEGORY TABLE
S60A
S61A
IS FUNCTIONAL UNIT CLASSIFICATION THE SAME, AND IS THERE CORRESPONDING FUNCTIONAL UNIT NUMBER?
YES
NO
S62
INCREASING LOGICAL INSTRUCTION POINTER BY 1
S63
LOGICAL SLOT POINTER < MAXIMUM VALUE?
NO
YES
ERROR
S70
S71
IS BASIC INSTRUCTION ASSIGNED TO ASSIGNABLE LOGICAL INSTRUCTION UNIT HAVING LOWER NUMERAL?
NO
ERROR
YES
S72
ASSIGNING BASIC INSTRUCTION
S73
INCREASING LOGICAL INSTRUCTION SLOT POINTER BY 1
S74
LAST BASIC INSTRUCTION IN VLIW INSTRUCTION?
YES
S75
INSTRUCTION SLOT CAN BE ASSIGNED
NO
S76
INCREASING PHYSICAL INSTRUCTION SLOT POINTER BY 1
A: TO BE REPEATED FOR ALL INSTRUCTION SLOTS
S54
TOO MANY BASIC INSTRUCTIONS IN VLIW INSTRUCTION
S55

FIG.29

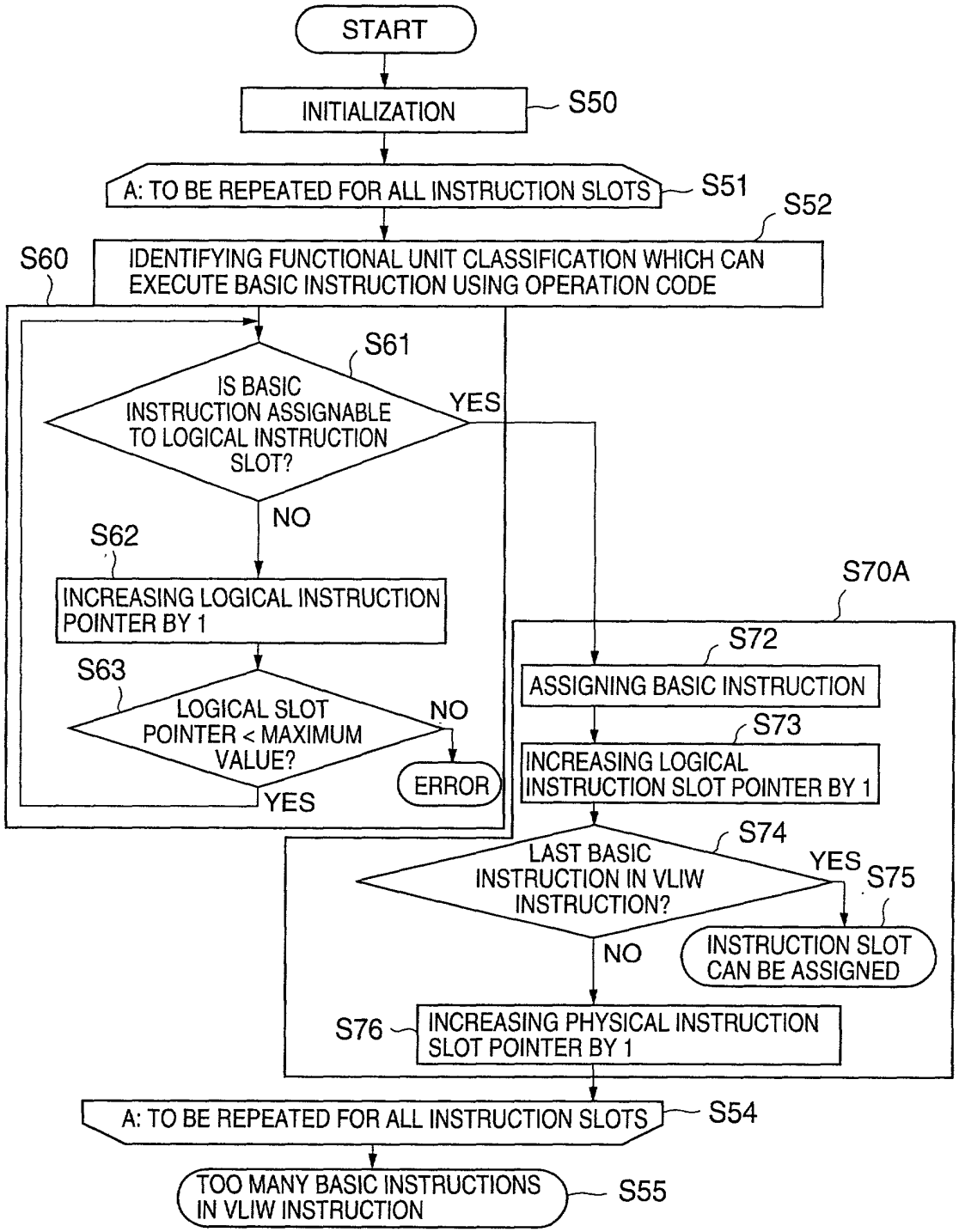

START
INITIALIZATION
S50
A: TO BE REPEATED FOR ALL INSTRUCTION SLOTS
S51
S52
S60
IDENTIFYING FUNCTIONAL UNIT CLASSIFICATION WHICH CAN EXECUTE BASIC INSTRUCTION USING OPERATION CODE
S61
IS BASIC INSTRUCTION ASSIGNABLE TO LOGICAL INSTRUCTION SLOT?
YES
NO
S62
INCREASING LOGICAL INSTRUCTION POINTER BY 1
S63
LOGICAL SLOT POINTER < MAXIMUM VALUE?
NO
YES
ERROR
S70A
S72
ASSIGNING BASIC INSTRUCTION
S73
INCREASING LOGICAL INSTRUCTION SLOT POINTER BY 1
S74
LAST BASIC INSTRUCTION IN VLIW INSTRUCTION?
YES
S75
INSTRUCTION SLOT CAN BE ASSIGNED
NO
S76
INCREASING PHYSICAL INSTRUCTION SLOT POINTER BY 1
A: TO BE REPEATED FOR ALL INSTRUCTION SLOTS
S54
TOO MANY BASIC INSTRUCTIONS IN VLIW INSTRUCTION
S55

FIG.30

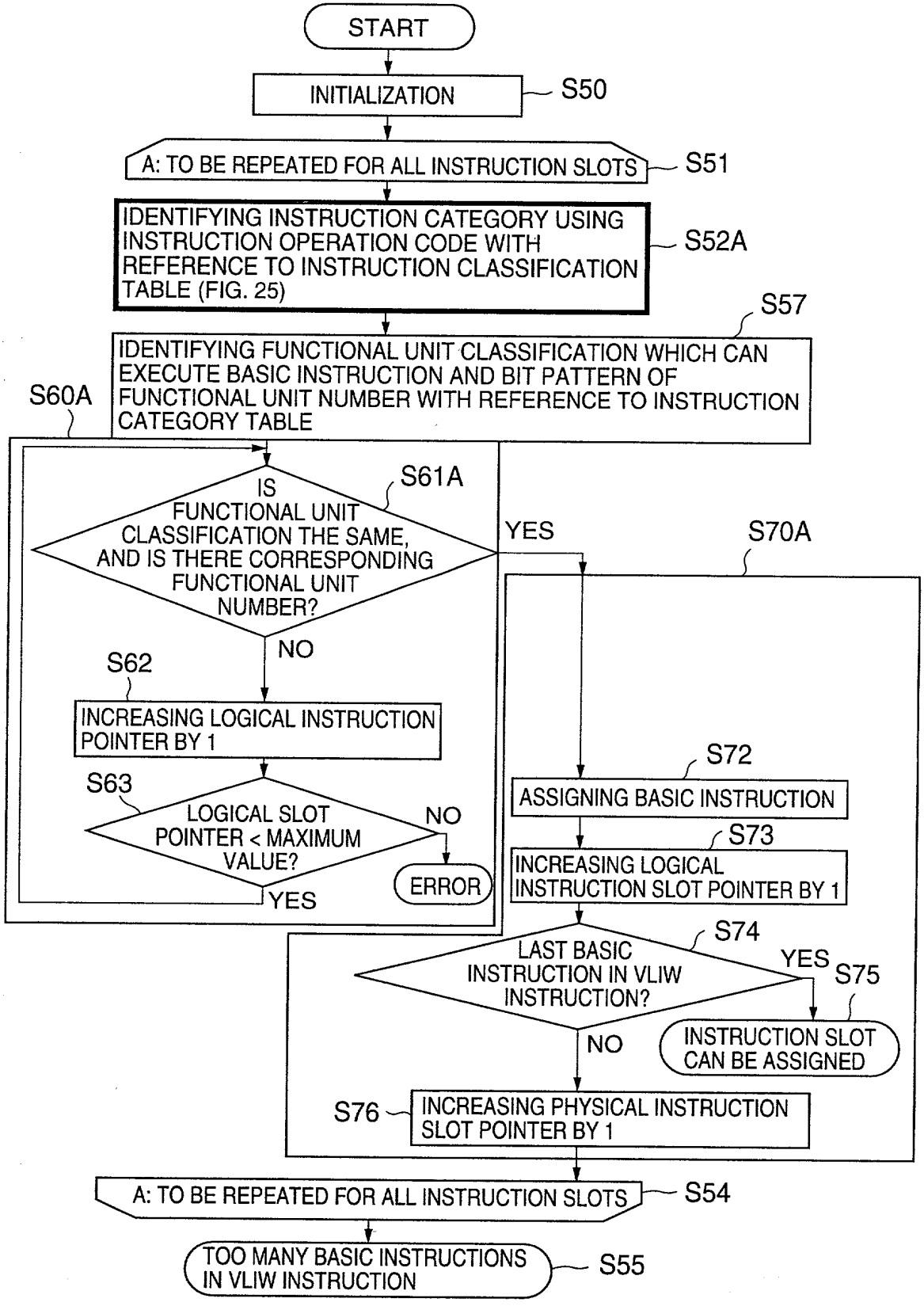

START
INITIALIZATION
S50
A: TO BE REPEATED FOR ALL INSTRUCTION SLOTS
S51
IDENTIFYING INSTRUCTION CATEGORY USING INSTRUCTION OPERATION CODE WITH REFERENCE TO INSTRUCTION CLASSIFICATION TABLE (FIG. 25)
S52A
S57
IDENTIFYING FUNCTIONAL UNIT CLASSIFICATION WHICH CAN EXECUTE BASIC INSTRUCTION AND BIT PATTERN OF FUNCTIONAL UNIT NUMBER WITH REFERENCE TO INSTRUCTION CATEGORY TABLE
S60A
S61A
IS FUNCTIONAL UNIT CLASSIFICATION THE SAME, AND IS THERE CORRESPONDING FUNCTIONAL UNIT NUMBER?
YES
NO
S62
INCREASING LOGICAL INSTRUCTION POINTER BY 1
S63
LOGICAL SLOT POINTER < MAXIMUM VALUE?
NO
YES
ERROR
S70A
S72
ASSIGNING BASIC INSTRUCTION
S73
INCREASING LOGICAL INSTRUCTION SLOT POINTER BY 1
S74
LAST BASIC INSTRUCTION IN VLIW INSTRUCTION?
YES
S75
INSTRUCTION SLOT CAN BE ASSIGNED
NO
S76
INCREASING PHYSICAL INSTRUCTION SLOT POINTER BY 1
A: TO BE REPEATED FOR ALL INSTRUCTION SLOTS
S54
TOO MANY BASIC INSTRUCTIONS IN VLIW INSTRUCTION
S55

FIG.31

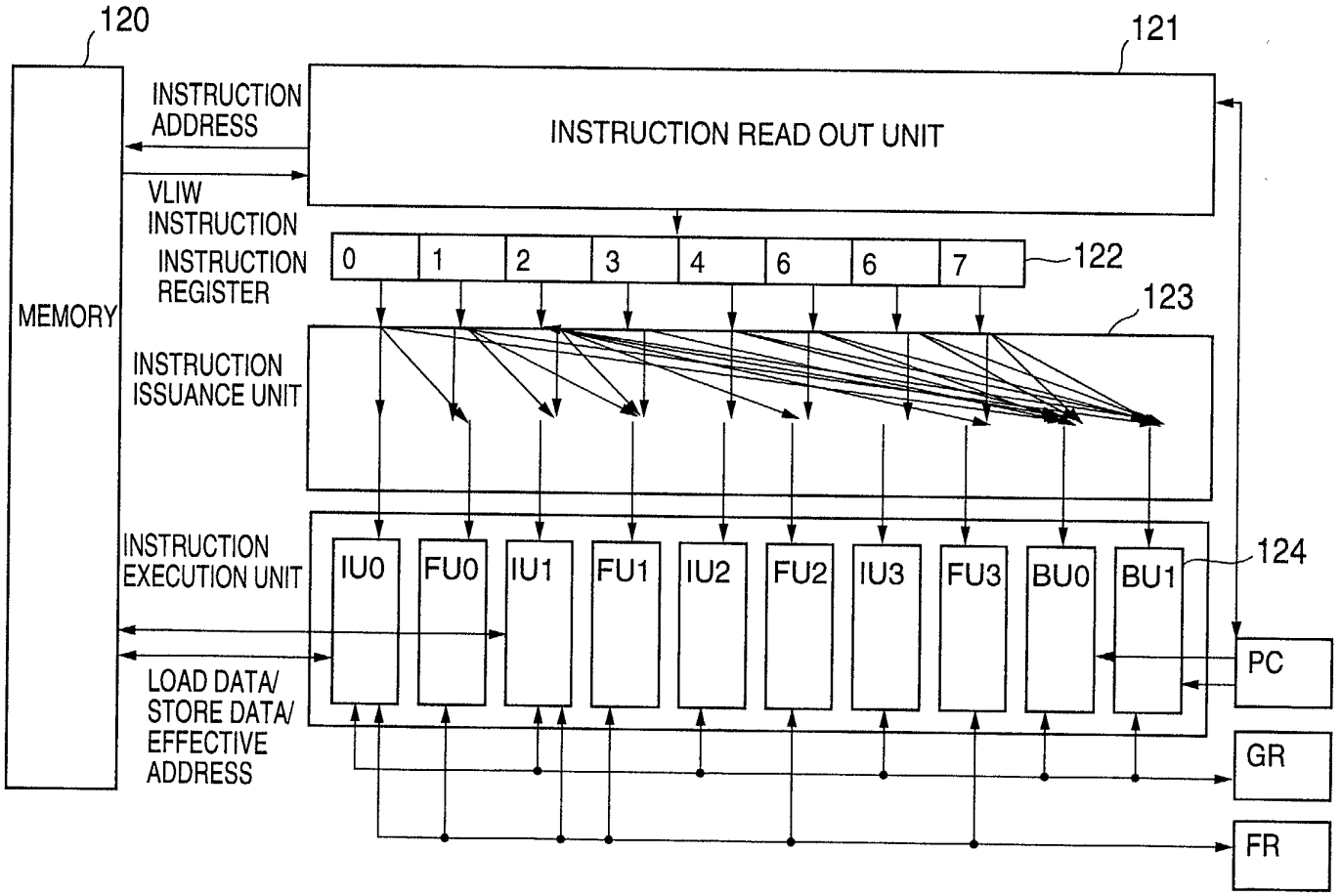

120
121
MEMORY
INSTRUCTION ADDRESS
INSTRUCTION READ OUT UNIT
VLIW INSTRUCTION
INSTRUCTION REGISTER
0
1
2
3
4
6
6
7
122
123
INSTRUCTION ISSUANCE UNIT
INSTRUCTION EXECUTION UNIT
IU0
FU0
IU1
FU1
IU2
FU2
IU3
FU3
BU0
BU1
124
PC
GR
FR
LOAD DATA/ STORE DATA/ EFFECTIVE ADDRESS

FIG.32

INSTRUCTION SLOT 0	INSTRUCTION SLOT 1	INSTRUCTION SLOT 2	INSTRUCTION SLOT 3	INSTRUCTION SLOT 4	INSTRUCTION SLOT 5	INSTRUCTION SLOT 6	INSTRUCTION SLOT 7
I0	F0	I1	F1	I2	F2	I3	F3
I0	F0	I1	F1	I2	F2	I3	B0
I0	F0	I1	F1	I2	F2	I3	
I0	F0	I1	F1	I2	F2	F3	B0
I0	F0	I1	F1	I2	F2	F3	
I0	F0	I1	F1	I2	F2	B0	B1
I0	F0	I1	F1	I2	F2	B0	
I0	F0	I1	F1	I2	F2		
I0	F0	I1	F1	I2	I3	B0	B1
I0	F0	I1	F1	I2	I3	B0	
I0	F0	I1	F1	I2	I3		
I0	F0	I1	F1	F2	F3	B0	B1
I0	F0	I1	F1	F2	F3	B0	
I0	F0	I1	F1	F2	F3		
I0	F0	I1	F1	I2	B0	B1	
I0	F0	I1	F1	I2	B0		
I0	F0	I1	F1	I2			
I0	F0	I1	F1	F2	B0	B1	
I0	F0	I1	F1	F2	B0		
I0	F0	I1	F1	F2			
I0	F0	I1	I2	I3	B0	B1	
I0	F0	I1	I2	I3	B0		
I0	F0	I1	I2	I3			
I0	F0	F1	F2	F3	B0	B1	
I0	F0	F1	F2	F3	B0		
I0	F0	F1	F2	F3			
I0	F0	I1	F1	B0	B1		
I0	F0	I1	F1	B0			
I0	F0	I1	F1				
I0	F0	I1	I2	B0	B1		
I0	F0	I1	I2	B0			
I0	F0	I1	I2				
I0	F0	F1	F2	B0	B1		
I0	F0	F1	F2	B0			
I0	F0	F1	F2				
I0	F0	I1	I2	B0	B1		
I0	F0	I1	I2	B0			
I0	F0	I1	I2				
F0	F1	F2	F3	B0	B1		
F0	F1	F2	F3	B0			

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FIG. 33

F0	F1	F2	F3				
I0	I1	I2	I3	B0	B1		
I0	I1	I2	I3	B0			
I0	I1	I2	I3				
I0	F0	I1	B0	B1			
I0	F0	I1	B0				
I0	F0	I1					
I0	F0	F1	B0	B1			
I0	F0	F1	B0				
I0	F0	F1					
F0	F1	F2	B0	B1			
F0	F1	F2	B0				
F0	F1	F2					
I0	I1	I2	B0	B1			
I0	I1	I2	B0				
I0	I1	I2					
I0	F0	B0	B1				
I0	F0	B0					
I0	F0						
F0	F1	B0	B1				
F0	F1	B0					
F0	F1						
I0	I1	B0	B1				
I0	I1	B0					
I0	I1						
I0	B0	B1					
I0	B0						
I0							
F0	B0	B1					
F0	B0						
F0							
B0	B1						
B0							

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FIG.34

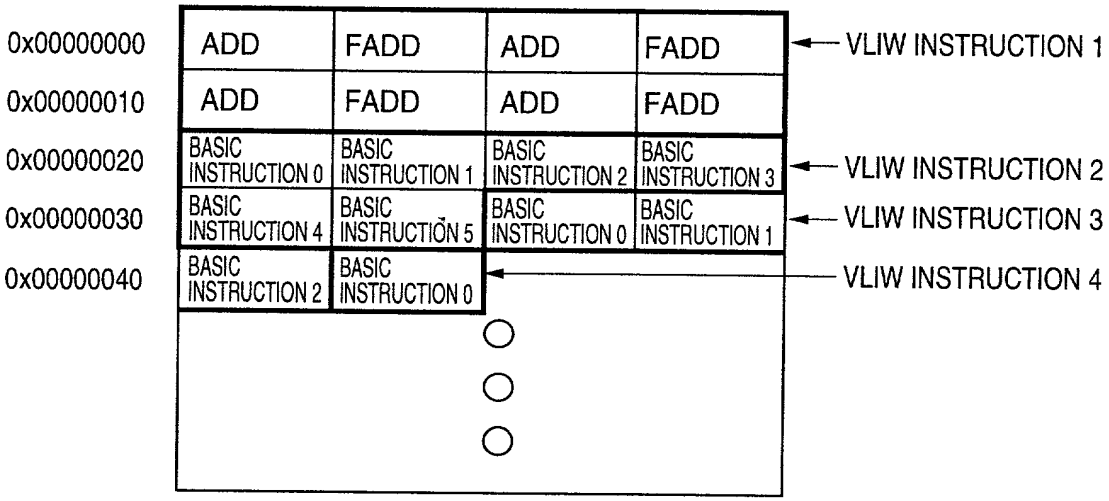
0x00000000
0x00000010
0x00000020
0x00000030
0x00000040
ADD
FADD
ADD
FADD
ADD
FADD
ADD
FADD
BASIC INSTRUCTION 0
BASIC INSTRUCTION 1
BASIC INSTRUCTION 2
BASIC INSTRUCTION 3
BASIC INSTRUCTION 4
BASIC INSTRUCTION 5
BASIC INSTRUCTION 0
BASIC INSTRUCTION 1
BASIC INSTRUCTION 2
BASIC INSTRUCTION 0
VLIW INSTRUCTION 1
VLIW INSTRUCTION 2
VLIW INSTRUCTION 3
VLIW INSTRUCTION 4

FIG. 35

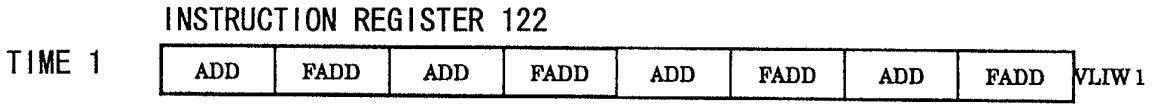
INSTRUCTION REGISTER 122
TIME 1
ADD
FADD
ADD
FADD
ADD
FADD
ADD
FADD
VLIW 1

FIG.36

INSTRUCTION OPERATION CODE	FUNCTIONAL UNIT CLASSIFICATION	FUNCTIONAL UNIT NUMBER OF EACH FUNCTIONAL UNIT CLASSIFICATION			
		0	1	2	3
ADD	IU	○	○	○	○
FADD	FU	○	○	○	○
BRA	BU	○	○	—	—

IU : EXECUTABLE BY INTEGER UNIT

FU : EXECUTABLE BY FLOATING UNIT

BU : EXECUTABLE BY BRANCH UNIT

○ : ASSIGNABLE

— : NOT ASSIGNABLE

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FIG.37

LOGICAL INSTRUCTION SLOT	ASSIGNABLE FUNCTIONAL UNIT CLASSIFICATION			FUNCTIONAL UNIT NUMBER OF EACH FUNCTIONAL UNIT CLASSIFICATION			
	IU	FU	BU	0	1	2	3
0	○	—	—	○	—	—	—
1	—	○	—	○	—	—	—
2	○	—	—	—	○	—	—
3	—	○	—	—	○	—	—
4	○	—	—	—	—	○	—
5	—	○	—	—	—	○	—
6	○	—	—	—	—	—	○
7	—	○	—	—	—	—	○
8	—	—	○	○	—	—	—
9	—	—	○	—	○	—	—

○ : ASSIGNABLE

— : NOT ASSIGNABLE

FIG.38

INSTRUCTION OPERATION CODE	INSTRUCTION CATEGORY
ADD	I_1
FADD	F_1
BRA	B_1

I_1 : INTEGER CATEGORY 1

F_1 : FLOATING CATEGORY 1

B_1 : BRANCH CATEGORY 1

FIG.39

INSTRUCTION CATEGORY	FUNCTIONAL UNIT CLASSIFICATION	FUNCTIONAL UNIT NUMBER OF EACH FUNCTIONAL UNIT CLASSIFICATION			
		0	1	2	3
I_1	IU	○	○	—	—
F_1	FU	○	○	—	—
B_1	BU	○	○	—	—

○ : EXECUTABLE — : NOT EXECUTABLE

FIG.40

LOGICAL INSTRUCTION SLOT	ASSIGNABLE FUNCTIONAL UNIT CLASSIFICATION			FUNCTIONAL UNIT NUMBER OF EACH FUNCTIONAL UNIT CLASSIFICATION			
	IU	FU	BU	0	1	2	3
0	○	—	—	○	—	—	—
1	—	○	—	○	—	—	—
2	○	—	—	—	○	—	—
3	—	○	—	—	○	—	—
4	—	—	○	○	—	—	—
5	—	—	○	—	○	—	—

○ : EXECUTABLE — : NOT EXECUTABLE

FIG.41

INSTRUCTION OPERATION CODE	INSTRUCTION CATEGORY
ADD	I_1
FADD	F_1
BRA	B_1

I_1 : INTEGER CATEGORY 1

F_1 : FLOATING CATEGORY 1

B_1 : BRANCH CATEGORY 1

FIG.42

INSTRUCTION CATEGORY	FUNCTIONAL UNIT CLASSIFICATION	FUNCTIONAL UNIT NUMBER OF EACH FUNCTIONAL UNIT			
		0	1	2	3
I_1	IU	○	○	—	—
F_1	FU	○	○	—	—
B_1	BU	○	○	—	—

○ : ASSIGNABLE

— : NOT ASSIGNABLE

FIG.43

LOGICAL INSTRUCTION UNIT	ASSIGNABLE FUNCTIONAL UNIT CLASSIFICATION			FUNCTIONAL UNIT NUMBER OF EACH FUNCTIONAL CLASSIFICATION			
	IU	FU	BU	0	1	2	3
0	○	—	—	○	—	—	—
1	—	○	—	○	—	—	—
2	○	—	—	—	○	—	—
3	—	○	—	—	○	—	—
4	○	—	—	—	—	○	—
5	—	○	—	—	—	○	—
6	○	—	—	—	—	—	○
7	—	○	—	—	—	—	○
8	—	—	○	○	—	—	—
9	—	—	○	—	○	—	—

○ : ASSIGNABLE

— : NOT ASSIGNABLE